CLAIMS

What is claimed is:

1. A method to forward network data in a data processing system, comprising:

(a) receiving network data;

(b) separating the network data into portions which will be modified and into portions which will not be modified;

(c) storing both portions of the network data in a local memory;

(d) forwarding the modifiable portions of the data to a cache associated with a processing element requesting at least the modifiable portion of the data;

(e) determining a destination of the modifiable portion;

(f) modifying the modifiable portions within the requesting processing element; and

(g) writing back the modified portion of the network data to the destination bypassing the local memory.

2. The method of claim 1, wherein the modifiable portion of the network data is a packet header of one network protocol which is modified to that of another network protocol.

3. The method of claim 2 wherein one and/or another network protocol is ATM.

4. The method of claim 2 wherein one and/or another network protocol is ethernet.

5. The method of claim 2 wherein one/and or another network protocol is PPP, point-to-point protocol.

6. The method of claim 2 wherein one/and or another network protocol is IP, internet protocol.

7. The method of claim 2, further comprising:
   (a) translating an address if the requesting processing element and the destination have different addresses of the local memory.

8. The method of claim 1, wherein the modification comprises updating an address to that of the destination.

9. The method of claim 1, wherein the modification occurs in a network processor.

10. The method of claim 1, wherein the modification occurs in a local processing element.

11. The method of claim 1, wherein the modification occurs in an embedded processor in an application specific integrated circuit, ASIC.

12. An apparatus for data communications, comprising:

(a) a network interface through which to receive incoming data comprised of at least one packet, the data packet having a modifiable portion and a portion that need not be modified;

(b) a local memory connected to the network interface, the local memory for receiving the data and storing the modifiable portion from the portion that need not be modified;

(c) a modifier which updates the modifiable portion of the data packet;

(d) a bus interface; and

(e) an interconnect fabric connected to the bus interface by which to forward the modifiable portion and the portion of the data that need not be modified to its destination.

13. The apparatus of claim 12, wherein the incoming data is digital electrical and/or optical data.

14. The apparatus of claim 12, wherein the incoming data is analog electrical and/or optical data.

15. A memory bypass mechanism, comprising:

(a) means to receive optical and/or digital data;

(b) means to separate the received data into a modifiable portion and a non-modifiable portion;

(c) means to store the received data in a first memory;

(d) means to forward the modifiable portion of the data to a modifying means;

(e) means to forward the non-modifiable portion to a destination;

(f) means to modify the modifiable portion; and

(g) means to forward the modified portion of data directly to its destination bypassing storing the modified portion in the first memory.

16. The memory bypass mechanism of claim 15, wherein the modifiable portion of the received data is a header stating a network protocol of the data and/or a destination address of the received data.

17. The memory bypass mechanism of claim 16, wherein the received header is of a first network protocol and the modified header is of a second network protocol.

18. The memory bypass mechanism of claim 17, wherein the first and second network protocols are selected from the group consisting of: asynchronous transfer mode, ethernet, Internet protocol, and Point-to-Point protocol.

19. The memory bypass mechanism of claim 15, wherein the modifying means is a processing element in a network processor.

20. The memory bypass mechanism of claim 19, wherein the destination is a different processing element in the network processor.

21. The memory bypass mechanism of claim 15, wherein the destination is a second memory.